PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Supp. 12½ Requ. for Recon. 1/8/02 A. Walk

In re the Application of

Hutter et al. (TI-27203)

Serial No. 09/276,780 Group Art Unit: 2825

Filed: March 25, 1999 Examiner: Luu

For: Merged Bipolar and CMOS Circuit and Method

REQUEST FOR RECONSIDERATION

Commissioner for Patents

Washington, DC 20231

Dear Sir:

In response to the Office Action mailed April 11, 2001, reconsideration of this application is requested.

Claims 1 through 5 remain in this case.

The allowance of claims 2 through 5 is noted.

Claim 1 was rejected under §102(b) as anticipated by the Liao et al. reference.[1] The Examiner asserted that the reference teaches the forming of a base region (24) of a bipolar transistor and a p-well (24) of an n-channel MOS transistor in a single implantation step,[2] and the forming of a collector contact well and an n-well of a p-channel MOS transistor in a single implantation step.[3]

[1] U.S. Patent No. 5,407,841 to Liao et al.

[2] Office Action of April 11, p. 2.

[3] *Id.*

Applicants respectfully traverse the rejection of claim 1, on the grounds that the teachings of the reference fall short of the requirements of the claim.

First, as noted above, the Examiner asserted that element 24 of the Liao et al. reference corresponds to a base region in a bipolar transistor. Applicants respectfully traverse the rejection on this basis, on the grounds that region 24 cannot serve as a base region in any bipolar transistor region of the disclosed structure. Referring to Figure 2 of the Liao et al. reference, the vertical NPN device region (third from the left) includes no portion of region 24; rather, the unlabeled portion that underlies regions 20, 22 for the vertical NPN device is n-type epitaxial silicon.[4] Accordingly, there is no portion of the vertical NPN device region corresponding to the base region that is formed by the same single implant as well 24 in the NMOS device (10). Regarding the vertical PNP device, region 24 is in fact present. However, because region 24 is p-type,[5] this region 24 cannot serve as the base region for vertical PNP device 6, simply because a PNP device requires an n-channel base region. Instead, the base region of vertical PNP device 6 of the reference is formed by a separate and subsequent implant,[6] which is a different implant from that used to form p-well 24 in the NMOS device.[7] Therefore, to the extent that the rejection of claim 1 is based on the characterization of the Liao et al. reference as teaching that the same implant as used to form p-well 24 also forms a base region in a bipolar device, Applicants submit that the rejection is in error.

Applicants respectfully submit that the Liao et al. reference fails to disclose the formation of a base region in a bipolar transistor with the same single implant as that used to form a p-well in an NMOS device as required by claim 1, because the Liao et al. reference instead teaches the formation of its base regions with implants separate from those used to form the p-well. The base region of the PNP device (6) of the Liao et al. reference cannot be formed with the same implant as used to form the p-well (24) in the NMOS region, because the n-type base region of a PNP transistor is necessarily of different conductivity type than a p-well. Regarding the NPN device disclosed by the

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[4] Liao et al., *supra*, column 4, lines 32 through 34; Figure 8.
[5] Liao et al., *supra*, column 4, lines 38 through 42.
[6] Liao et al., *supra*, column 7, lines 15 through 18.
[7] Liao et al., *supra*, column 4, lines 38 through 42.

Liao et al. reference, its external base region (62) is formed with the same implant as used to form source/drain regions in the PMOS device,[8] and its P-base implant (66) is performed after the formation of the PMOS source/drains and external p-type base region, by a separate masked implant.[9] Accordingly, the two portions of the base region of the NPN device of the Liao et al. references are formed by implants that are separate from, and indeed subsequent to, the formation of the p-well in the NMOS device. Applicants therefore respectfully submit that the Liao et al. reference falls short of the requirements of claim 1, because there is no disclosure in the reference of the forming, in a single implantation step, a base region of a bipolar transistor and a p-well of an n-channel MOS transistor, as required by the claim.

Applicants therefore respectfully traverse the §102 rejection of claim 1 in this application.

Applicants further respectfully submit that there is no suggestion from the prior art to modify the teachings of the Liao et al. reference in such a manner as to reach claim 1. The Liao et al. reference itself provides no such suggestion in this regard. The Prengle et al. reference teaches that the intrinsic base region (69) of its bipolar transistor is formed by a masked implant, during which time the MOS transistors are masked from receiving the implant;[10] accordingly, the Prengle et al. references lacks any suggestion to modify the teachings of the Liao et al. reference so as to reach claim 1. The other references either do not discuss the process steps for forming a BiCMOS structure, or disclose masked implants for the base region that are separate from the implant that forms the p-well in an NMOS device.[11] Accordingly, because the prior art provides no suggestion to modify the teachings of the Liao et al. reference in such a manner as to reach claim 1, Applicants submit that claim 1 is not only novel, but is also patentably distinct, over the Liao et al. reference, whether taken individually or in combination with the other prior art of record in this case.

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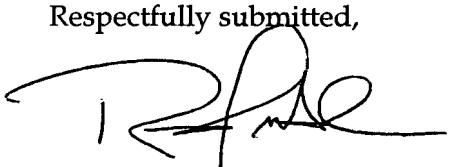
[8] Liao et al., *supra*, column 7, lines 5 through 8; column 8, lines 4 through 6.
[9] Liao et al., *supra*, column 7, lines 18 through 20.
[10] U.S. Patent No. 5,171,702 to Prengle et al., column 8, lines 18 through 29.
[11] *See*, e.g., Havemann et al., "Process Integration Issues for Submicron BiCMOS Technology", *Solid State Technology* (June 1992), pp. 71 through 76, at Table I, p. 73.

For all of the above reasons, Applicants respectfully submit that all claims in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,



Rodney M. Anderson
Registry No. 31,939
Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.
12160 Abrams Road, Suite 111
Dallas, Texas 75243
(972) 664-9554

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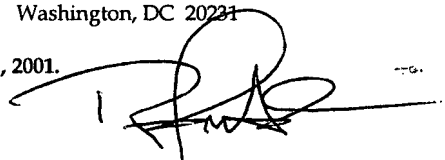

Rodney M. Anderson
Registry No. 31,939